Title: Digital Noise Generators for ADC Built-In Self-Test

Objectives:

This project proposal can be divided in two different tasks: the study and implementation of digital noise generators, and its application to the built-in self-test (BIST) of integrated analog-to-digital converters (ADCs).

The noise generators will be based in random number generation, a well-studied area with a large number of algorithms already proposed. The random number generators can be divided in two classes, the true and the pseudorandom. The first class is based in measures of some physical phenomena. The second type of generators, the pseudorandom, are based in mathematical algorithms that produce long sequences of apparently random numbers which are in fact completely determined by an initial value, known as a seed. Both classes of random number generation should be evaluated.

These random generators will be used in the implementation of Gaussian and uniform digital noise generators. Despite the large number of algorithms already proposed, there is no single algorithm that generates random numbers good enough for any kind of application. This issue is the core of this work, which comprises the implementation of digital noise generators (with a Gaussian and a uniform distribution) and its evaluation in the aim of an ADC BIST solution. The digital noise generators will be implemented with a hardware description language in field programmable gate arrays (FPGAs).

The proposed BIST techniques will be based in the histogram test and should be adapted for the two classes of noise generators. The BIST solution for the uniform noise generator is usually simpler as its implementation does not require complex functions and/or large tables. Before its development in FPGAs, a simulation setup should be implemented (in Python or Matlab environments) and evaluated. For that goal, several digital noise generators, digital-to-analogue converters (DACs) needed to provide an analogue continuous-time input to the ADCs and ADCs with different architectures and resolutions should be also implemented. The noise generators’ algorithms with the accuracy needed for the BIST should be implemented in a FPGA and evaluated to choose the best solution for each type of noise.

Finally, a BIST solution for each type of noise generator (only one noise generator should selected by the user in the beginning of a test), will be implemented at the same FPGA and will be used to test commercial ADCs with different architectures and resolutions. In the final setup, these two noise generators and its BIST solutions should be optimized both in speed and occupied resources in the FPGA implementation.

Framework:

The use of BIST techniques based on the histogram method to test high-resolution ADCs has been studied in the last years. These techniques accelerate the test time and
alleviate the dependency on high cost test equipment, without compromising the quality of the test. One of the important issues of the BIST is the accuracy of the generator used as stimulus. Different type of analogue generators were implemented in integrated circuit namely, sinusoidal, ramp and noise generators, but there are some drawbacks in their application to ADC BIST. The sinusoidal and the ramp generators are difficult to implement with the accuracy needed. The implementation of integrated analogue noise generators is easier but the generators work at low amplitude values, which difficult its application in ADC histogram tests.

There are several advantages of using a Gaussian noise as stimulus signal: only the first order statistics are relevant for the characterization; a disturbance in the generated noise variance only induces a gain error; not being a periodic signal relaxes the need for circular sampling; the time required for ADC test is quite reduced. So, the Gaussian noise generator is probably the best stimulus for on-chip full-speed characterization of ADCs through histogram tests.

Due to the limited range of applications, uniform noise generators are not so well studied. By not being used to study physical phenomena they can only be used in very special applications as the one proposed in this project.

The digital implementation of noise generators for an ADC BIST, usually leads to larger power dissipations and die areas since a DAC and a low-pass filter are required to provide an analogue continuous-time output. But when compared to the analogue solution it has two important advantages: the circuits needed for the noise generators are simpler; and the distribution of amplitudes is not limited by the circuit supply voltage (it only depends on the DAC).

Tasks:

This project proposal comprises the following tasks:

- Selection of the noise generation algorithms to be evaluated.
- Proposal of ADC BIST solutions for the two type of noise generators (Gaussian and uniform).
- Simulation in a suitable programming language of the digital BIST solutions and of several ADCs (and DACs to provide an analogue continuous-time input) with different architectures and resolutions.
- Implementation in a FPGA of a set of digital noise generators to be evaluated in the BIST simulation environment. All the firmware will be developed with a hardware description language.
- Selection of the best two classes of noise generators and its optimization in speed and space occupation in the FPGA. The BIST solutions for each type of noise generators should be also implemented in the same FPGA.
- Evaluation of the BIST setup in the test of commercial ADCs with different architectures and resolutions.
The work will be developed in the Group of Electronics and Instrumentation (Faculty of Sciences of the University of Lisbon - FCUL) laboratory.

This plan will follow the doctoral PhD Plan in Engineering Physics of the FCUL, with an appropriate academic component of the training, containing mandatory courses (Doctoral Seminars I, II and III, and Research Seminar) and courses to enhance training in Electronics and Instrumentation and Computational Physics.


University to which the thesis project will be presented: University of Lisbon

DAEPHYS Scientific Domain in which the project fits: Engineering Physics

Thematic area of DAEPHYS: Instrumentation

Connection of the project to the thematic areas of DAEPHYS:

The project proposal fits in all subareas of the theme Instrumentation area of DAEPHYS since testing is one of the most important fields in instrumentation. The project proposal can be divided in two areas: digital noise generators and BIST of ADCs. The noise generators can be applied to all those subareas since they can be used for testing and calibration of instruments and/or measurement techniques and, in the case of the Gaussian generators also for the theoretical study of physical phenomena. The ADCs allow the acquisition of physical signals and its conversion to a digital signal for further processing. The quality of an instrument is highly dependent of the quality and resolution of its converters, and ADCs with 10 or more bits of resolution need to have BIST solutions. Finally, the developed BIST solutions may be used to inspire the improvement of other measurement techniques.

Candidate profile: Master in Engineering Physics, in Physics or equivalent, with experience in Electronics and Instrumentation.

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